

REMARKS

Claims 54 and 62 have been amended to make it clear that the recited "main portion" is the "main plate portion". Also, "finger" has been corrected to "finger portion" in Claim 54. Dependent Claims 123 - 130 have been added to claim the invention with more particularity¹. No claims have been canceled. Accordingly, Claims 17 - 130 are now pending.

The logical structure of the claims is now somewhat difficult to see due to the various amendments by which new claims have been added. To facilitate examination of the application, enclosed as Appendix A is a list in which the claims are grouped in logical, rather than numerical, order. Method claims having structure counterparts are generally located directly after the structure counterparts in Appendix A.

Claims 17 - 31, 38 - 67, 69, 71 - 98, 100 - 113, and 115 - 122 have been rejected under 35 USC 102(e) as anticipated by Litwin et al. ("Litwin"), U.S. Patent 6,100,770. Claims 32 - 37, 68, 99, and 114 have been rejected under 35 USC 103(a) as obvious based on Litwin in view of Misu et al. ("Misu"), Japanese Patent Publication 7-226643. These rejections are respectfully traversed.

The present rejections contain a clear procedural error which was pointed out in the Response submitted 17 June 2003, which was again pointed out in the Amendment submitted 14 January 2004 because the error was not corrected in the Office Action mailed 16 September 2003, which was temporarily corrected in the Office Action mailed 21 April 2004, but which has been re-introduced in the present Office Action. The procedural error is that dependent Claim 70 has been rejected on the basis of narrower art, a single reference, than the art, a combination of references, used to reject independent Claim 32 from which Claim 70 depends.

More particularly, the first page of the present Office Action indicates that Claim 70 is a rejected claim. The claim listings presented in the Office Action for the claims rejected under 35 USC 102(a) as anticipated by Litwin and for the claims rejected under 35 USC 103(a) as obvious based on Litwin and Misu do not include Claim 70. However, the Examiner states on page 5 of the Office Action that "claim 70 is now rejected under 35 USC

¹ Non-amended claims presented in the application as filed were parenthetically indicated by the term "Previously presented" in earlier amendments and are parenthetically indicated here by the term "Original" so as to conform better with the requirements of 37 CFR 1.121.

102(e) and not 103(a)". Also, the rationale presented in the Office Action for the anticipation rejection refers to Claim 70 as if it were being rejected as anticipated by Litwin. In the anticipation-rejection material bridging pages 2 and 3 of the Office Action, the Examiner alleges that "Regarding claims 17-19, . . . 70-72, and 79-83, Litwin discloses . . .". Thus, it clearly seems that Claim 70 is now being rejected as anticipated by Litwin.

Claim 70 depends, as indicated above, from independent Claim 32 which has been rejected as obvious based on Litwin and Misu. As is required for a dependent claim, dependent Claim 70 further limits Claim 32. Hence, the art used to reject dependent Claim 70 must be at least as broad as, and cannot correctly be narrower than, the art used to reject Claim 32. It is procedurally incorrect for Claim 70 to be rejected as anticipated by Litwin while Claim 32 is simultaneously rejected as obvious based on Litwin and Misu. In the event that this application goes to appeal, it is respectfully requested that the Examiner correct the procedural error in order to simplify the issues for appeal.

For the purpose of responding to the prior art rejections, Applicant's Attorney hereafter treats Claim 70 as if it has been rejected as obvious under 35 USC 103(a) based on Litwin and Misu.

Insofar as Claims 17 - 31, 38 - 67, 69, and 71 - 88 are concerned, the present anticipation rejection substantially repeats the anticipation rejection presented in the Office Action mailed 17 March 2003, repeated in the September 2003 Office Action, and again repeated in the April 2004 Office Action.

Reasons were presented in the Amendment submitted 19 December 2002 as to why Claims 17 - 31, 38 - 67, 69, and 71 - 88 are patentable over Litwin. Those reasons were largely repeated in the June 2003 Response. In light of the minor revisions made to independent Claims 17 and 71 in the January 2004 Amendment, additional reasons were presented in the January 2004 Amendment as to why Claims 17 and 71 and their dependent claims are patentable over Litwin. To reduce repetitiveness, all of these reasons were largely incorporated by reference into the Amendment submitted 21 July 2004.

As was the case with the March 2003, September 2003, and April 2004 Office Actions, nothing in the present Office Action shows why any of the previously presented reasons is wrong or why any of Claims 17 - 31, 38 - 67, 69, and 71 - 88 is unpatentable based on Litwin. Accordingly, the anticipation rejection of Claims 17 - 31, 38 - 67, 69, and 71 - 88

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is traversed for substantially the same reasons presented in the December 2002 Amendment, the June 2003 Response, the January 2004 Amendment, and the July 2004 Amendment.

In explaining why Claims 17, 18, 71, and 72 were revised in the January 2004 Amendment, Applicant's Attorney first presented the following Litwin material on pages 15 - 17 of the January 2004 Amendment²:

Litwin discloses several modes for operating the varactor of Fig. 1. A first operational mode, referred to here as mode 1, is disclosed at col. 5, lines 21 - 58, with respect to the schematic varactor diagram of Fig. 4 corresponding to Fig. 1. In mode 1, a voltage is applied between electrodes C_A and C_B to produce a depletion layer below the gate dielectric layer that underlies gate electrode 16. Electrode C_A is connected to source 13 and drain 14 while electrode C_B is connected to gate electrode 16. Litwin states that the capacitance between electrodes C_A and C_B is the series combination of gate dielectric capacitance C_{OX} and depletion layer capacitance C_D . Adjusting the voltage between electrodes C_A and C_B causes depletion layer capacitance C_D to change so as to change the overall capacitance between electrodes C_A and C_B .

Litwin does not disclose any electrode connection to well 12 in mode 1. Hence, well 12 is presumably floating, i.e., not connected to any external electrode, in mode 1.

A second operational mode, referred to here as mode 2, is disclosed at col. 5, lines 59 - 64. In mode 2, depletion layer capacitance C_D is controlled by applying a suitable variable potential to well 12 while electrodes C_A and C_B are maintained at respective fixed potentials. Again, electrode C_A is connected to source 13 and drain 14 while electrode C_B is connected to gate electrode 16.

A third operational mode is disclosed at col. 5, lines 64 - 67, where Litwin states that "a fixed potential is applied to one of the electrodes C_A or C_B the other electrode is connected to the well 12 and the device is controlled by a suitable voltage applied to the well". The third operational mode divides into two sub-modes referred to here as sub-mode 3A and sub-mode 3B. In sub-mode 3A, a fixed potential is applied to electrode C_A connected to source 13 and drain 14, and a variable potential is applied to electrode C_B connected to well 12. In sub-mode 3B, a fixed potential is applied to electrode C_B

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² In the July 2004 Amendment, Applicant's Attorney incorrectly identified the pages at which this material appears in the January 2004 Amendment. As indicated here, this material appears at pages 15 - 17 of the January 2004 Amendment rather than at pages 20 - 22 as specified in the July 2004 Amendment. Also, in repeating this material from the January 2004 amendment, the subscripting of reference symbols was lost in the first paragraph of the material as repeated in the July 2004 Amendment. The subscripting has been corrected in the first paragraph of the repeated material here.

connected to gate electrode 16, and a variable potential is applied to electrode C_A connected to well 12.

Litwin is unclear as to whether the connection of electrode C_A or C_B to well 12 in the third mode is alternative to, or in addition to, the earlier-identified C_A and C_B connections. In preparing the December 2002 Amendment and June 2003 Response, Applicant's Attorney had concluded that Litwin means the alternative situation. The following connections then occur in sub-mode 3A: electrode C_A is connected to source 13 and drain 14, electrode C_B is connected to well 12, and gate electrode 16 is unconnected. This electrical arrangement is referred to here as mode 3A1. For the alternative situation, sub-mode 3B similarly becomes sub-mode 3B1 in which electrode C_A is connected to well 12, electrode C_B is connected to gate electrode 16, and source 13 and drain 14 are unconnected.

Applicant's Attorney reviewed Litwin with Applicant in the course of preparing this amendment. In that review, Applicant was of the view that Litwin means the additional, rather than alternative, situation. Sub-mode 3A then has the following connections referred to here as mode 3A2: electrode C_A is connected to source 13 and drain 14, and electrode C_B is connected to gate electrode 16 and well 12. Similarly, sub-mode 3B has the following connections referred to here as mode 3B2: electrode C_A is connected to source 13, drain 14, and well 12, and electrode C_B is connected to gate electrode 16.

Applicant's Attorney then summarized Litwin's possible operational modes in the paragraph bridging pages 16 and 17 of the January 2004 Amendment. In so doing, Applicant's Attorney incorrectly specified that electrodes C_A and C_B are respectively at fixed and variable potentials in mode 3B2 rather than being respectively at variable and fixed potentials as described earlier in the quoted material. As so corrected, the electrical connections for the six possible operational modes in Litwin are summarized below:

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Summary of Litwin's Possible Operational Modes

- Mode 1:
- a. Source 13 and drain 14 connected to electrode C_A
 - b. Gate electrode 16 connected to electrode C_B with variable potential applied between electrodes C_A and C_B whereby potential between source 13 and gate electrode 16 is variable
 - c. Well 12 unconnected
- Mode 2:
- a. Source 13 and drain 14 connected to electrode C_A at fixed potential
 - b. Gate electrode 16 connected to electrode C_B at fixed potential
 - c. Well 12 connected to further electrode at variable potential whereby (a) potential between source 13 and well 12 is variable and (b) potential between gate electrode 16 and well 12 is variable
- Mode 3A1:
- a. Source 13 and drain 14 connected to electrode C_A at fixed potential
 - b. Gate electrode 16 unconnected
 - c. Well 12 connected to electrode C_B at variable potential whereby potential between source 13 and well 12 is variable
- Mode 3A2:
- a. Source 13 and drain 14 connected to electrode C_A at fixed potential
 - b. Gate electrode 16 connected to electrode C_B at variable potential whereby potential between source 13 and gate electrode 16 is variable
 - c. Well 12 connected to electrode C_B whereby (a) potential between gate electrode 16 and well 12 is zero and (b) potential between source 13 and well 12 is variable and equals potential between source 13 and gate electrode 16
- Mode 3B1:
- a. Source 13 and drain 14 unconnected
 - b. Gate electrode 16 connected to electrode C_B at fixed potential
 - c. Well 12 connected to electrode C_A at variable potential whereby potential between gate electrode 16 and well 12 is variable
- Mode 3B2:
- a. Source 13 and drain 14 connected to electrode C_A at variable potential
 - b. Gate electrode 16 connected to electrode C_B at fixed potential whereby potential between source 13 and gate electrode 16 is variable
 - c. Well 12 connected to electrode C_A whereby (a) potential between source 13 and well 12 is zero and (b) potential between gate electrode 16 and well 12 is variable and equals potential between gate electrode 16 and source 13

As mentioned on page 17 of the January 2004 Amendment, only four of the six operational modes given here actually apply to the varactor device of Figs. 1 and 4 since Litwin means the two sub-modes of the third operational mode to be either modes 3A1 and 3B1 or modes 3A2 and 3B2. With the electrode connections appropriately adjusted, the device of Figs. 1 and 4 of Litwin can thus be operated in any of modes 1, 2, 3A1, and 3B1 or in any of modes 1, 2, 3A2, and 3B2 depending on whether Litwin means modes 3A1 and 3B1 or modes 3A2 and 3B2.

As pointed out in the above material repeated from pages 15 - 17 of the January 2004 Amendment, Litwin discloses at col. 5, lines 21 - 58, that the controlled variable capacitance provided by the varactor device of Figs. 1 and 4 for operation in mode 1 is the series combination of gate dielectric capacitance C_{OX} and depletion layer capacitance C_D taken between electrodes C_A and C_B . Since electrodes C_A and C_B are connected respectively to plate region 13 and gate electrode 16 in mode 1, the variable capacitance provided by the device of Figs. 1 and 4 in mode 1 is the series combination of capacitances C_{OX} and C_D taken between plate region 13 and gate electrode 16.

Nothing in Litwin discloses or suggests that the variable capacitance provided by the device of Figs. 1 and 4 is anything but the series combination of capacitances C_{OX} and C_D between plate region 13 and gate electrode 16 when the device of Figs. 1 and 4 is operated in any of the other modes. In describing the other operational modes at col. 5, lines 59 - 67, Litwin does not mention any other way for taking the variable capacitance during operation in any of these other modes. This indicates that Litwin intends to take the variable capacitance between plate region 13 and gate electrode 16 in all of the operational modes.

Gate electrode 16 is unconnected in mode 3A1 while plate region 13 is unconnected in mode 3B1. As a result, operating the device of Figs. 1 and 4 in mode 3A1 or 3B1 would not yield the series combination of gate dielectric capacitance C_{OX} and depletion layer capacitance C_D as the device's controlled variable capacitance. This indicates that Litwin does not intend to operate in mode 3A1 or 3B1. That is, Litwin's disclosure at col. 5, lines 64 - 67, that "Alternatively, a fixed potential is applied to one of the electrodes C_A or C_B the other electrode is connected to the well 12 and the device is controlled by a suitable voltage applied to the well" means modes 3A2 and 3B2 in which plate region 13 and gate electrode 16 are respectively connected to electrodes C_A and C_B . The four operational modes most likely contemplated by Litwin thus consist of modes 1, 2, 3A2, and 3B2. Nevertheless, modes 3A1 and 3B1 are considered below in showing why the anticipation and obvious rejections should be withdrawn.

Turning to independent Claims 17 and 71, they are repeated below:

17. A structure comprising a varactor which comprises:

a plate region and a body region of a semiconductor body, the body region being of a first conductivity type, the plate region being of a second

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conductivity type opposite to the first conductivity type, the plate and body regions meeting each other to form a p-n junction;

a plate electrode and a body electrode respectively connected to the plate and body regions, the plate electrode being at a plate-to-body bias voltage relative to the body electrode;

a dielectric layer situated over the semiconductor body and contacting the body region; and

a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, the gate electrode being at a gate-to-body bias voltage relative to the body electrode, the gate-to-body voltage being maintained approximately constant at a non-zero value as the plate-to-body voltage is varied.

71. A method comprising:

providing a varactor which comprises (a) a plate region and a body region of a semiconductor body, (b) a plate electrode and a body electrode respectively connected to the plate and body regions, (c) a dielectric layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions meeting each other to form a p-n junction;

applying (a) a plate-to-body bias voltage between the plate and body electrodes and (b) a gate-to-body bias voltage between the gate and body electrodes; and

varying the plate-to-body voltage while maintaining the gate-to-body voltage approximately constant at a non-zero value to cause an inversion layer that meets the plate region to selectively appear and disappear in the body region below the gate electrode.

Importantly, Claims 17 and 71 both require that the gate-to-body voltage be maintained approximately constant at a non-zero value as the plate-to-body voltage is varied. This requirement is not met by any of Litwin's devices in any of Litwin's six possible operational modes.

More specifically, the Examiner appears to have made the following analogies between the features of Litwin's varactor devices and the features of the present claims, including Claims 17 and 71:

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a. Source 13 in the device of Figs. 1 and 4 corresponds to the "plate region" of the claims;

b. Gate electrode 16 in the device of Figs. 1 and 4 corresponds to the "gate electrode" of the claims; inasmuch as the claims do not recite any separate electrode connected to the gate electrode, the Examiner presumably also views any electrode, such as electrode C_B, connected to gate electrode 16 as being part of the "gate electrode" of the claims;

c. Well region 12 in the device of Figs. 1 and 4 corresponds to the "body region" of the claims;

d. The voltage between plate region 13 and body region 12 in the device of Figs. 1 and 4 corresponds to the "plate-to-body voltage" of the claims; and

e. The voltage between gate electrode 16 and body region 12 in the device of Figs. 1 and 4 corresponds to the "gate-to-body voltage" of the claims.

Using these analogies, the subject matter of each of Claims 17 and 71 differs from the device in Figs. 1 and 4 of Litwin as operated in any of the six possible modes 1, 2, 3A1, 3A2, 3B1, and 3B2 for the following reasons.

In mode 1 of Litwin, a variable potential is applied between (a) electrode C_A connected to plate region 13 and (b) electrode C_B connected to gate electrode 16. Hence, the "gate-to-plate" voltage between gate electrode 16 and plate region 13 varies in mode 1. Body region 12 is unconnected in mode 1. This enables the voltage at body region 12 to float, i.e., vary, as the "gate-to-plate" voltage varies. The voltage limitations of mode 1 could arise from any of the following three scenarios:

I. The voltage at plate region 13 varies while the voltage at gate electrode 16 is constant so that the "gate-to-plate" voltage varies due to the variance of the voltage at plate region 13;

II. The voltage at gate electrode 16 varies while the voltage at plate region 13 is constant so that the "gate-to-plate" voltage varies due to the variance of the voltage at gate electrode 16; and

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III. The voltages at plate region 13 and gate electrode 16 both vary, but in different ways, so that the "gate-to-plate" voltage varies.

Taking note of the fact that the voltage at body region 12 floats and thus varies in mode 1, the "gate-to-body" voltage between gate electrode 16 and body region 12 in scenario I of mode 1 varies because the voltage at gate electrode 16 is constant. Consequently, scenario I of mode 1 does not meet the requirement of Claims 17 and 71 that the gate-to-body voltage be maintained approximately constant (at a non-zero value) as the plate-to-body voltage is varied.

In scenario II of mode 1, the voltage at gate electrode 16 varies while the voltage at plate region 13 is constant. As a result, the voltage at gate electrode 16 in scenario II would have to vary approximately the same as the voltage at body region 12 for the "gate-to-body" voltage to be approximately constant. However, nothing in Litwin discloses, inherently requires, or in any way suggests that the voltage at gate electrode 16 varies approximately the same as the voltage at body region 12 in mode 1. Scenario II of mode 1 does not meet the requirement of Claims 17 and 71 that the gate-to-body voltage be maintained approximately constant as the plate-to-body voltage is varied.

With respect to scenario III in which the voltages at plate region 13 and gate electrode 16 both vary but in different ways, the voltage at gate electrode 16 would likewise have to vary approximately the same as the voltage at body region 12 for the "gate-to-body" voltage to be approximately constant in scenario III. Again, nothing in Litwin discloses, inherently requires, or in any way suggests that the voltage at gate electrode 16 varies approximately the same as the voltage at body region 12 in mode 1. Scenario III of mode 1 does not meet the requirement of Claims 17 and 71 that the gate-to-body voltage be maintained approximately constant as the plate-to-body voltage is varied.

As far as Applicant's Attorney can determine, the voltage limitations of mode 1 can arise only in scenarios I - III. Since none of scenarios I - III meets the requirement of Claims 17 and 71 that the gate-to-body voltage be maintained approximately constant as the plate-to-body voltage is varied, neither of Claims 17 and 17 is anticipated by Litwin's device in Figs. 1 and 4 when it operates in mode 1.

In mode 2 of Litwin, plate region 13 and gate electrode 16 are respectively connected to electrodes C_A and C_B at (different) fixed potentials. Body region 12 in mode 2 is

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connected to a further electrode at a variable potential. Since the voltages at gate electrode 16 and plate region 13 are thereby both constant while the voltage at body region 12 varies, the "gate-to-body" voltage between gate electrode 16 and body region 12 in mode 2 varies as the "plate-to-body" voltage between plate region 13 and body region 12 varies. Litwin's modification of the device of Figs. 1 and 4 to operate in mode 2 does not meet the requirement of Claims 17 and 71 that the gate-to-body voltage be maintained approximately constant as the plate-to-body voltage is varied. Neither of Claims 17 and 71 is anticipated by Litwin's device in Figs. 1 and 4 as modified to operate in mode 2.

Next consider the four possible versions of Litwin's third operational mode. In mode 3A1, plate region 13 is connected to electrode C_A at a fixed potential. Body region 12 in mode 3A1 is connected to electrode C_B at a variable potential. Inasmuch as the voltage at plate region 13 is thereby constant while the voltage at body region 12 varies, the "plate-to-body" voltage between plate region 13 and body region 12 varies in mode 3A1.

Gate electrode 16 is unconnected in mode 3A1. The voltage at gate electrode 16 thus floats, or varies, in mode 3A1 as the "plate-to-body" voltage varies. For the "gate-to-body" voltage between gate electrode 16 and body region 12 to be approximately constant in mode 3A1 as the "plate-to-body" voltage varies, the voltage at gate electrode 16 would have to vary approximately the same as the voltage at body region 12. As is the case with scenarios II and III of mode 1, nothing in Litwin discloses, inherently requires, or in any way suggests that the voltage at gate electrode 16 in the device of Figs. 1 and 4 varies approximately the same as the voltage at body region 12 for operation in mode 3A1. Mode 3A1 does not meet the requirement of Claims 17 and 71 that the gate-to-body voltage be maintained approximately constant as the plate-to-body voltage is varied. Neither Claim 17 nor Claim 71 is anticipated by Litwin via operation of the device of Figs. 1 and 4 in mode 3A1.

In mode 3A2, plate region 13 is connected to electrode C_A at a fixed potential while gate electrode 16 and body region 12 are both connected to electrode C_B at a variable potential. Because gate electrode 16 and body region 12 are connected together through electrode C_B , the voltage at gate electrode 16 is the same as the voltage at body region 12. Consequently, the "gate-to-body" voltage between gate electrode 16 and body region 12 in mode 3A2 is zero. Operation of the device of Figs. 1 and 4 in mode 3A2 fails to meet the requirement of Claims 17 and 71 that the gate-to-body voltage be maintained approximately

constant at a non-zero value as the plate-to-body voltage is varied. Neither of Claims 17 and 71 is anticipated by Litwin via operation of the device of Figs. 1 and 4 in mode 3A2.

In mode 3B1, plate region 13 is unconnected. This enables the voltage at plate region 13 to float. Gate electrode 16 is connected to electrode C_A at a fixed potential in mode 3B1 while body region 12 is connected to electrode C_B at a variable potential. That is, the voltage at gate electrode 16 is constant while the voltage at body region 12 is variable.

Also, the "plate-to-body" voltage between plate region 13 and body region 12 in mode 3B1 varies as long as the voltage at body region 12 differs from the voltage at plate region 13. As a result, the "gate-to-body" voltage between gate electrode 16 and body region 12 in mode 3B1 varies as the "plate-to-body" voltage varies. Operation of the device of Figs. 1 and 4 in mode 3B1 does not meet the requirement of Claims 17 and 71 that the gate-to-body voltage be maintained approximately constant as the plate-to-body voltage is varied. Neither of Claims 17 and 71 is anticipated by Litwin via operation of the device of Figs. 1 and 4 in mode 3B1.

In mode 3B2, plate region 13 and body region 12 are both connected to electrode C_A at a variable potential. Hence, the voltage at plate region 13 in mode 3B2 is the same as the voltage at body region 12. This causes the "plate-to-body" voltage between plate region 13 and body region 12 to be zero in mode 3B2.

Gate electrode 16 in mode 3B2 is connected to electrode C_B at a fixed potential. Since the voltage at gate electrode 16 is thereby constant in mode 3B2 while the voltage at body region 12 varies, the "gate-to-body" voltage between gate electrode 16 and body region 12 varies in mode 3B2. Due to this and to the fact that the "plate-to-body" voltage is constant at zero in mode 3B2, operation of the device of Figs. 1 and 4 in mode 3B2 fails to meet the requirement of Claims 17 and 71 that the gate-to-body voltage be maintained approximately constant as the plate-to-body voltage is varied. Neither Claim 17 nor Claim 71 is anticipated by Litwin via operation of the device of Figs. 1 and 4 in mode 3B2.

The net result is that neither of Claims 17 and 71 is anticipated by Litwin for operation of the device of Figs. 1 and 4 in any of the six possible modes 1, 2, 3A1, 3A2, 3B1, and 3B2. Likewise, operation of any of Litwin's other devices in a mode corresponding to any of modes 1, 2, 3A1, 3A2, 3B1, and 3B2 would not meet the requirement of Claims 17 and 71 that the gate-to-body voltage be maintained approximately constant at a non-zero

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value as the plate-to-body voltage is varied. Accordingly, Litwin does not anticipate Claim 17 or 71 for operation any of Litwin's devices in any of modes 1, 2, 3A1, 3A2, 3B1, and 3B2 or in a mode corresponding to any of modes 1, 2, 3A1, 3A2, 3B1, and 3B2.

On page 5 of the present Office Action in apparent response to the comments made by Applicant's Attorney in the July 2004 Amendment, the Examiner states that:

Applicant argues that claims 17 and 71 each require that the gate-to-body voltage be maintained approximately constant. However, as applicant identifies in operational mode 2, the well region could have a distinct electrode that is not shown in the figures. This is also indicated at column 5, line 62. Earlier in column 5, it is stated that different voltages can be applied to the gate and plate region. Since the body region could have a distinct control electrode other than the plate and gate electrodes, then it follows that the well and the plate voltages can be different, while the plate voltage varies. This is the same as mode 1 as identified by applicant, and also indicated at column 5 of Litwin, lines 24-26.

Applicant's Attorney does not see how these comments support the Examiner's contention that Litwin anticipates Claims 17 and 71.

It is true that, as occurs in operational mode 2, body region 12 of the device in Figs. 1 and 4 of Litwin can be provided with an electrode distinct from electrodes C_A and C_B. It is also true that, as occurs in scenarios I and III of operational mode 1, the voltages at plate region 13 and gate electrode 16 of Litwin's device in Figs. 1 and 4 can be different while the voltage at plate region 13 varies. However, Claims 17 and 71 place specific restrictions on the gate-to-body and plate-to-body voltages, namely that the gate-to-body voltage be maintained approximately constant at a non-zero value as the plate-to-body voltage is varied. As demonstrated above, none of Litwin's devices when operated in any of the six possible operational modes 1, 2, 3A1, 3A2, 3B1, and 3B2 (for the device of Figs. 1 and 4) or (for any of Litwin's other devices) in an operational mode corresponding to any of these six modes meets these voltage restrictions. Litwin therefore does not anticipate Claim 17 or 71.

Nothing in Litwin would provide a person skilled in the art with any suggestion or incentive for maintaining the "gate-to-body" voltage between gate electrode 16 and body region 12 constant at a non-zero value in the device of Figs. 1 and 4 as the "plate-to-body" voltage between plate region 13 and body region 12 is varied. Nor would anything in Litwin furnish a person skilled in the art with any suggestion or incentive for maintaining the "gate-

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to-body" voltage constant at a non-zero value in any of Litwin's other devices as the "plate-to-body" voltage is varied. Claims 17 and 71 are thus patentable over Litwin.

Repeating what was stated on page 26 of the July 2004 Amendment, independent Claims 23, 38, 63, and 79 are patentable over Litwin for the reasons presented in the December 2002 Amendment and the June 2003 Response. The Examiner is again referred to those two documents for these reasons.

No rebuttal has been presented in the September 2003 Office Action (issued in response to the December 2002 Amendment), in the April 2004 Office Action (issued in response to the June 2003 Response), or in the present Office Action to the reasons presented in the December 2002 Amendment and in the June 2003 Response as to why Claims 23, 38, 63, and 79 are patentable over Litwin. Nor does Applicant's Attorney see any reason(s) why any of Claims 23, 38, 63, and 79 is not patentable over Litwin. Accordingly, Claims 23, 38, 63, and 79 are patentable over Litwin for the reasons presented in the December 2002 Amendment and in the June 2003 Response.

Claims 18 - 22, 24 - 31, 39 - 62, 64 - 67, 69, 72 - 78, and 80 - 94 all variously depend (directly or indirectly) from independent Claims 17, 23, 38, 63, 71, and 79. The same applies to new Claims 123 - 128. As a result, dependent Claims 18 - 22, 24 - 31, 39 - 62, 64 - 67, 69, 72 - 78, 80 - 94, and 123 - 128 are variously patentable over Litwin for the same reasons as Claims 17, 23, 38, 63, 71, and 79.

As pointed out in the December 2003 Amendment, in the June 2003 Response, in the January 2004 Amendment, and in the July 2004 Amendment, Litwin does not disclose the further limitation of any of dependent Claims 18, 20, 29, 39, 40, 43, 53, 61, 67, 69, 72, 73, and 83. As similarly pointed out in the July 2004 Amendment, Litwin does not disclose the further limitation of dependent Claim 89 or 92. Litwin also does not disclose the further limitation of new dependent Claim 123 or 126.

The reasons why Litwin fails to disclose the further limitations of Claims 89, 92, 123, and 126 are presented below after dealing with the similar reasons why independent Claims 95 and 109 are patentable over Litwin. In any event, separate grounds are present for allowing Claims 18, 20, 29, 39, 40, 43, 53, 61, 67, 69, 72, 73, 83, 89, 92, 123, and 126 over Litwin. The same applies to Claims 90, 91, 93, 94, 124, 125, 127, and 128 since they variously depend from Claims 89, 92, 123, and 126.

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With respect to dependent Claims 20, 29, 39, 40, and 73 (and also dependent Claim 30), the Examiner alleges on page 3 of the Office Action that "capacitance dependency on the plate area, an inversion layer in the body region, and dependence of the capacitance on the inversion area all are inherent properties of the device [of Litwin]".

Claims 20, 29, 39, 40, and 73 all recite further limitations that depend on providing the controlled variable capacitance between the plate and body regions. As mentioned above, the controlled variable capacitance of Litwin's device in Figs. 3 and 4 is only disclosed in Litwin as being provided between plate region 13 and gate electrode 16 so as to be the series combination of gate dielectric capacitance C_{OX} and depletion layer capacitance C_D . Nowhere does Litwin disclose that the variable capacitance of the device of Figs. 1 and 4 is taken between plate region 13 and body region 12. Litwin does not disclose the further limitation of any of Claims 20, 29, 39, 40, and 73. For this reason, Claims 20, 29, 39, 40, and 73 are separately allowable over Litwin.

Turning to independent Claims 95 and 109 submitted in the July 2004 Amendment, Claims 95 and 109 are repeated below:

95. A method comprising:

selecting a varactor which comprises (a) a plate region and a body region of a semiconductor body, (b) a dielectric layer situated over the semiconductor body and contacting the body region, (c) a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, and (d) a plate electrode and a body electrode respectively connected to the plate and body regions, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions meeting each other to form a p-n junction and extending to a primary surface of the semiconductor body, the plate region occupying a lateral plate area along the primary surface, a field insulating region extending into the semiconductor body along the primary surface to define a semiconductor island laterally surrounded by the field insulating region and substantially fully occupied by material of the plate and body regions, the semiconductor island occupying a lateral island area along the primary surface, the varactor having a maximum capacitance dependent on the island area; and

adjusting the plate and island areas to control the minimum and maximum capacitances of the varactor.

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109. A structure comprising:

a varactor comprising (a) a plate region and a body region of a semiconductor body, (b) a plate electrode and a body electrode respectively connected to the plate and body regions, (c) a dielectric layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions meeting each other to form a p-n junction and extending to a primary surface of the semiconductor body, a field insulating region extending into the semiconductor body along the primary surface to define a semiconductor island laterally surrounded by the field insulating region and substantially fully occupied by material of the plate and body regions; and

electronic circuitry having a capacitance signal path for receiving the varactor to enable the circuitry to perform an electronic function dependent on the varactor, the plate and body electrodes being situated in the capacitance signal path.

Importantly, Claims 95 and 109 each require that the plate and body regions extend "to a primary surface of the semiconductor body" and that a field insulating region extend "into the semiconductor body along the primary surface to define a semiconductor island laterally surrounded by the field insulating region and substantially fully occupied by material of the plate and body regions".

With regard to Claim 95 (along with twelve other claims), the Examiner alleges on pages 3 and 4 of the present Office Action that:

... Litwin discloses in figure 8 (note that the plate and body regions here correspond to the same regions as figure 4, that is one of the regions 73 or 74 is a plate region and n-well 72 is the body region), a field insulating region extending into the semiconductor body (although the insulating film corresponding to the gates 76 is not numbered in this figure, it is present beneath the gate regions 76, along with the insulating film on the surface of the well region. See the description of figures 7 and 8, columns 7 and 8) along the primary surface to define a semiconductor island laterally surrounded by the field insulating region and substantially fully occupied by material of the plate and body regions, that is the material in regions 72, 73, and 74.

The Examiner's contention that Fig. 8 of Litwin discloses a "field insulating region" extending into the semiconductor body along the primary surface to define a semiconductor

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island laterally surrounded by the field insulating region and substantially fully occupied by material 72, 73, and 74 of the plate and body regions is incorrect.

As shown in Fig. 8 of Litwin, regions 72 - 74 are laterally surrounded by a region labeled "71". At lines 59 - 65 of col. 7 and lines 8 - 11 of col. 8, Litwin discloses that region 71 is a p-type semiconductor substrate. Semiconductor material is not electrically insulating material. Semiconductor substrate 71 which laterally surrounds regions 72 - 74 in Fig. 8 of Litwin therefore does not constitute an electrically insulating region. Fig. 8 and the associated text in Litwin do not disclose the field insulating region of Claim 95. Consequently, Litwin does not anticipate Claim 95.

On page 4 of the present Office Action, the Examiner refers specifically to Fig. 6 (of Litwin) in connection with Claim 109 (and twelve other claims). Fig. 6 of Litwin is a circuit diagram of a voltage controlled oscillator ("VCO") that employs implementations of one of Litwin's varactor devices. No field insulating region of the type recited in Claim 109 is illustrated in Fig. 6. Nor does Litwin anywhere indicate that any of the varactor implementations employed in the VCO of Fig. 6 is provided with a field insulating region as recited in Claim 109. As with Claim 95, Fig. 8 and the associated text in Litwin do not disclose the field insulating region of Claim 109. Litwin thus does not anticipate Claim 109.

Claims 96 - 108 variously depend (directly or indirectly) from Claim 95. Claims 110 - 122 variously depend (directly or indirectly) from Claim 109. The same applies to new dependent Claims 129 and 130. Hence, dependent Claims 96 - 108, 110 - 122, 129, and 130 are patentable over Litwin for the same reasons as Claims 95 and 109.

Litwin does not disclose the further limitation of any of dependent Claims 96, 98, 100, 101, 110, 111, 113, 115, 116, 129, and 130. Separate grounds are thereby present for allowing Claims 96, 98, 100, 101, 110, 111, 113, 115, 116, 129, and 130 over Litwin. Claims 96 and 110, which both depend on taking the controlled variable capacitance between the plate and body regions, are separately allowable over Litwin for the same reasons, presented above, as Claims 20, 29, 39, 40, and 73.

Returning briefly to dependent Claims 89, 92, 123, and 126, each of Claims 89 and 92 recites that "the providing act includes providing a field insulating region extending into the semiconductor body along the primary surface to define a semiconductor island laterally surrounded by the field insulating region and substantially fully occupied by material of the

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plate and body regions". Each of Claims 123 and 126 similarly recites that the claimed structure includes "a field insulating region extending into the semiconductor body along the primary surface to define a semiconductor island laterally surrounded by the field insulating region and substantially fully occupied by material of the plate and body regions". For the reasons presented above in connection with Claims 95 and 109, Litwin does not disclose the field insulating region of any of Claims 89, 92, 123, and 126. This establishes the above-mentioned separate grounds for allowing Claims 89, 92, 123, and 126 over Litwin.

Applicant's Attorney is, as indicated above, treating dependent Claim 70 as if its rejection is an obviousness rejection based on Litwin and Misu. Subject to this, Claims 32 - 37, 68, and 70 are patentable over Litwin and Misu for the reasons presented in the June 2003 Response. These reasons were partially repeated in the January 2004 Amendment and augmented in the July 2004 Amendment.

No rebuttal has been presented in the present Office Action to the augmented reasons presented in the July 2004 Amendment as to why Claims 32 - 37, 68, and 70 are patentable over Litwin and Misu. Applicant's Attorney does not see any reason(s) why any of Claims 32 - 37, 68, and 70 is not patentable over Litwin and Misu. Accordingly, Claims 32 - 37, 68, and 70 are patentable over Litwin and Misu for the augmented reasons presented in the July 2004 Amendment to which the Examiner is referred.

As also pointed out in the June 2003 Response, in the January 2004 Amendment, and in the July 2004 Amendment, Litwin does not disclose the further limitation of dependent Claim 36 or 70. Consequently, these two dependent claims are separately allowable over Litwin and Misu.

In summary, all of pending Claims 17 - 130 have been shown to be patentable over the applied art. Accordingly, Claims 17 - 130 should be allowed so that the application may proceed to issue.

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APPENDIX A
CLAIMS 17 - 130, IN LOGICAL ORDER,
OF U.S. PATENT APPLICATION 09/903,059,
ATTORNEY DOCKET NO. NS-4971 US

17. A structure comprising a varactor which comprises:
a plate region and a body region of a semiconductor body, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions meeting each other to form a p-n junction;
a plate electrode and a body electrode respectively connected to the plate and body regions, the plate electrode being at a plate-to-body bias voltage relative to the body electrode;
a dielectric layer situated over the semiconductor body and contacting the body region;
and
a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, the gate electrode being at a gate-to-body bias voltage relative to the body electrode, the gate-to-body voltage being maintained approximately constant at a non-zero value as the plate-to-body voltage is varied.
69. A structure as in Claim 17 wherein an inversion layer that meets the plate region selectively appears and disappears in the body region below the gate electrode as the plate-to-body voltage is varied during operation of the varactor.
18. A structure as in Claim 17 further including componentry for maintaining the gate-to-body voltage approximately constant at the non-zero value.
19. A structure as in Claim 17 wherein the plate and body regions extend to a primary surface of the semiconductor body.
123. A structure as in Claim 19 further including a field insulating region extending into the semiconductor body along the primary surface to define a semiconductor island laterally surrounded by the field insulating region and substantially fully occupied by material of the plate and body regions.
124. A structure as in Claim 123 wherein the plate region is a substantially unitary region.

125. A method as in Claim 123 wherein the field insulating region substantially laterally surrounds at least one further semiconductor island occupied by material of the body region substantially up to the primary surface such that material of the body region extends continuously from each semiconductor island to each other semiconductor island.

20. A structure as in Claim 19 wherein the plate region occupies a lateral plate area along the primary surface, the varactor has a minimum capacitance dependent on the plate area, an inversion layer that meets the plate region selectively appears and disappears in the body region below the gate electrode under control of the plate and body electrodes, the inversion layer occupies a lateral inversion area along the primary surface, and the varactor has a maximum capacitance dependent on the inversion area in combination with the plate area.

21. A structure as in Claim 19 wherein the body region substantially laterally surrounds, and extends below substantially all of, the plate region.

22. A structure as in Claim 21 wherein the plate region comprises a main plate portion and at least one finger portion continuous with the main plate portion, extending laterally away from the main plate portion, and meeting the body region therealong.

54. A structure as in Claim 22 wherein each finger portion is of lesser average dimension perpendicular to that finger portion than is the main plate portion.

47. A structure as in Claim 17 further including electronic circuitry having a capacitance signal path for receiving the varactor to enable the circuitry to perform an electronic function dependent on the varactor, the plate and body electrodes being situated in the capacitance signal path.

48. A structure as in Claim 47 wherein the gate electrode is situated outside the capacitance signal path.

49. A structure as in Claim 47 wherein the circuitry comprises at least one additional region of the semiconductor body.

50. A structure as in Claim 47 wherein the circuitry comprises an inductor.

51. A structure as in Claim 17 further including electronic circuitry comprising an inductor situated in an inductance-capacitance signal path with the plate and body electrodes to form an oscillatory inductive-capacitive combination.

52. A structure as in Claim 51 wherein the gate electrode is situated outside the inductance-capacitance signal path.

53. A structure as in Claim 17 wherein a surface depletion region of the body region extends along the dielectric layer below the gate electrode and is spaced apart from a body contact portion of the body region, the body contact portion contacting the body electrode and being more heavily doped than the surface depletion region.

71. A method comprising:

providing a varactor which comprises (a) a plate region and a body region of a semiconductor body, (b) a plate electrode and a body electrode respectively connected to the plate and body regions, (c) a dielectric layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions meeting each other to form a p-n junction;

applying (a) a plate-to-body bias voltage between the plate and body electrodes and (b) a gate-to-body bias voltage between the gate and body electrodes; and

varying the plate-to-body voltage while maintaining the gate-to-body voltage approximately constant at a non-zero value to cause an inversion layer that meets the plate region to selectively appear and disappear in the body region below the gate electrode.

72. A method as in Claim 71 further including providing componentry for maintaining the gate-to-body voltage approximately constant at the non-zero value.

89. A method as in Claim 71 wherein:

the plate and body regions extend to a primary surface of the semiconductor body; and
the providing act includes providing a field insulating region extending into the semiconductor body along the primary surface to define a semiconductor island laterally

surrounded by the field insulating region and substantially fully occupied by material of the plate and body regions.

90. A method as in Claim 89 wherein the providing act includes configuring the plate region to be a substantially unitary region.

91. A method as in Claim 89 wherein the providing act includes configuring the field insulating region to substantially laterally surround at least one further semiconductor island occupied by material of the body region substantially up to the primary surface such that material of the body region extends continuously from each semiconductor island to each other semiconductor island.

73. A method as in Claim 71 wherein the plate and body regions extend to a primary surface of the semiconductor body, the plate region occupies a lateral plate area along the primary surface, the varactor has a minimum capacitance dependent on the plate area, the inversion layer occupies a lateral inversion area along the primary surface, and the varactor has a maximum capacitance dependent on the inversion area in combination with the plate area.

74. A method as in Claim 71 wherein the plate region comprises a main plate portion and at least one finger portion continuous with the main plate portion, extending laterally away from the main plate portion, and meeting the body region therealong.

75. A method as in Claim 71 further including providing electronic circuitry having a capacitance signal path for receiving the varactor to enable the circuitry to perform an electronic function dependent on the varactor, the plate and body electrodes being situated in the capacitance signal path.

76. A method as in Claim 75 wherein the gate electrode is situated outside the capacitance signal path.

77. A method as in Claim 71 further including providing electronic circuitry comprising an inductor situated in an inductance-capacitance signal path with the plate and body electrodes to form an oscillatory inductive-capacitive combination.

78. A method as in Claim 77 wherein the gate electrode is situated outside the inductance-capacitance signal path.

23. A structure comprising a varactor which comprises:

a plate region and a body region of a semiconductor body, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions meeting each other to form a p-n junction;

a plate electrode and a body electrode respectively connected to the plate and body regions, the plate electrode being at a plate-to-body bias voltage relative to the body electrode;

a dielectric layer situated over the semiconductor body and contacting the body region;
and

a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, the gate electrode being at a gate-to-body bias voltage relative to the body electrode, the gate-to-body voltage differing from the plate-to-body voltage, the gate-to-body voltage varying as a function of the plate-to-body voltage as the plate-to-body voltage is varied during operation of the varactor to cause an inversion layer that meets the plate region to selectively appear and disappear in the body region below the gate electrode.

24. A structure as in Claim 23 wherein the gate-to-body voltage varies approximately linearly with the plate-to-body voltage.

25. A structure as in Claim 23 wherein the gate-to-body voltage differs by approximately a constant non-zero amount from the plate-to-body voltage.

26. A structure as in Claim 23 further including componentry for causing the gate-to-body voltage to vary as a function of the plate-to-body voltage.

27. A structure as in Claim 26 wherein the componentry causes the gate-to-body voltage to vary approximately linearly with the plate-to-body voltage.

28. A structure as in Claim 23 wherein the plate and body regions extend to a primary surface of the semiconductor body.

126. A structure as in Claim 28 further including a field insulating region extending into the semiconductor body along the primary surface to define a semiconductor island laterally surrounded by the field insulating region and substantially fully occupied by material of the plate and body regions.

127. A structure as in Claim 126 wherein the plate region is a substantially unitary region.

128. A method as in Claim 126 wherein the field insulating region substantially laterally surrounds at least one further semiconductor island occupied by material of the body region substantially up to the primary surface such that material of the body region extends continuously from each semiconductor island to each other semiconductor island.

29. A structure as in Claim 28 wherein the plate region occupies a lateral plate area along the primary surface, the varactor has a minimum capacitance dependent on the plate area, the inversion layer occupies a lateral inversion area along the primary surface, and the varactor has a maximum capacitance dependent on the inversion area in combination with the plate area.

30. A structure as in Claim 28 wherein the body region substantially laterally surrounds, and extends below substantially all of, the plate region.

31. A structure as in Claim 30 wherein the plate region comprises a main plate portion and at least one finger portion continuous with the main plate portion, extending laterally away from the main plate portion, and meeting the body region therealong.

62. A structure as in Claim 31 wherein each finger portion is of lesser average dimension perpendicular to that finger portion than is the main plate portion.

55. A structure as in Claim 23 further including electronic circuitry having a capacitance signal path for receiving the varactor to enable the circuitry to perform an electronic function dependent on the varactor, the plate and body electrodes being situated in the capacitance signal path.

56. A structure as in Claim 55 wherein the gate electrode is situated outside the capacitance signal path.

57. A structure as in Claim 55 wherein the circuitry comprises at least one additional region of the semiconductor body.

58. A structure as in Claim 55 wherein the circuitry comprises an inductor.

59. A structure as in Claim 23 further including electronic circuitry comprising an inductor situated in an inductance-capacitance signal path with the plate and body electrodes to form an oscillatory inductive-capacitive combination.

60. A structure as in Claim 59 wherein the gate electrode is situated outside the inductance-capacitance signal path.

61. A structure as in Claim 23 wherein a surface depletion region of the body region extends along the dielectric layer below the gate electrode and is spaced apart from a body contact portion of the body region, the body contact portion contacting the body electrode and being more heavily doped than the surface depletion region.

79. A method comprising:

providing a varactor which comprises (a) a plate region and a body region of a semiconductor body, (b) a plate electrode and a body electrode respectively connected to the plate and body regions, (c) a dielectric layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions meeting each other to form a p-n junction;

applying (a) a plate-to-body bias voltage between the plate and body electrodes and (b) a gate-to-body bias voltage between the gate and body electrodes; and

varying (a) the plate-to-body voltage and (b) the gate-to-body voltage as a function of the plate-to-body voltage as the plate-to-body voltage is varied to cause an inversion layer that meets the plate region to selectively appear and disappear in the body region below the gate electrode.

80. A method as in Claim 79 wherein the gate-to-body voltage varies approximately linearly with the plate-to-body voltage.

81. A method as in Claim 79 further including providing componentry for causing the gate-to-body voltage to vary as a function of the plate-to-body voltage.
82. A method as in Claim 79 wherein the componentry causes the gate-to-body voltage to vary approximately linearly with the plate-to-body voltage.
92. A method as in Claim 79 wherein:
the plate and body regions extend to a primary surface of the semiconductor body; and
the providing act includes providing a field insulating region extending into the semiconductor body along the primary surface to define a semiconductor island laterally surrounded by the field insulating region and substantially fully occupied by material of the plate and body regions.
93. A method as in Claim 92 wherein the providing act includes configuring the plate region to be a substantially unitary region.
94. A method as in Claim 92 wherein the providing act includes configuring the field insulating region to substantially laterally surround at least one further semiconductor island occupied by material of the body region substantially up to the primary surface such that material of the body region extends continuously from each semiconductor island to each other semiconductor island.
83. A method as in Claim 79 wherein the plate and body regions extend to a primary surface of the semiconductor body, the plate region occupies a lateral plate area along the primary surface, the varactor has a minimum capacitance dependent on the plate area, the inversion layer occupies a lateral inversion area along the primary surface, and the varactor has a maximum capacitance dependent on the inversion area in combination with the plate area.
84. A method as in Claim 79 wherein the plate region comprises a main plate portion and at least one finger portion continuous with the main plate portion, extending laterally away from the main plate portion, and meeting the body region therealong.
85. A method as in Claim 79 further including providing electronic circuitry having a capacitance signal path for receiving the varactor to enable the circuitry to perform an electronic

function dependent on the varactor, the plate and body electrodes being situated in the capacitance signal path.

86. A method as in Claim 85 wherein the gate electrode is situated outside the capacitance signal path.

87. A method as in Claim 79 further including providing electronic circuitry comprising an inductor situated in an inductance-capacitance signal path with the plate and body electrodes to form an oscillatory inductive-capacitive combination.

88. A method as in Claim 87 wherein the gate electrode is situated outside the inductance-capacitance signal path.

32. A structure comprising:

a plate region and a body region of a semiconductor body, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions extending to a primary surface of the semiconductor body and meeting each other to form a p-n junction, the plate region comprising a main plate portion and a plurality of finger portions continuous with the main plate portion, extending laterally away from the main plate portion, and meeting the body region therealong, at least two of the finger portions extending longitudinally non-parallel to one another;

a dielectric layer situated over the semiconductor body and contacting the plate region;
and

a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region.

70. A structure as in Claim 32 further including a plate electrode and a body electrode respectively connected to the plate and body regions, an inversion layer that meets the plate region selectively appearing and disappearing in the body region below the gate electrode as a plate-to-body bias voltage applied between the plate and the body electrodes is varied during operation of the structure.

33. A structure as in Claim 32 wherein each finger portion is of lesser average dimension perpendicular to that finger portion than is the main plate portion.

34. A structure as in Claim 32 wherein the body region substantially laterally surrounds, and extends below substantially all of, the plate region including each finger portion.

35. A structure as in Claim 32 further including a field insulating region extending into the semiconductor body along its primary surface, the field insulating region laterally adjoining the body region.

36. A structure as in Claim 32 wherein two of the finger portions extend longitudinally largely perpendicular to each other.

37. A structure as in Claim 32 wherein there are at least four finger portions.

38. A method comprising:

selecting a varactor which comprises (a) a plate region and a body region of a semiconductor body, (b) a dielectric layer situated over the semiconductor body and contacting the body region, (c) a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, and (d) a plate electrode and a body electrode respectively connected to the plate and body regions, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions meeting each other to form a p-n junction and extending to a primary surface of the semiconductor body, the plate region occupying a lateral plate area along the primary surface, the varactor having a minimum capacitance dependent on the plate area, an inversion layer that meets the plate region selectively appearing and disappearing in the body region below the gate electrode as a plate-to-body bias voltage applied between the plate and body electrodes is varied during operation of the varactor, the inversion layer occupying a lateral inversion area along the primary surface, the varactor having a maximum capacitance dependent on the inversion area in combination with the plate area; and

adjusting the plate and inversion areas to control the minimum and maximum capacitances of the varactor.

39. A method as in Claim 38 wherein the minimum capacitance is approximately proportional to the plate area, and the maximum capacitance is approximately proportional to an accumulative combination of the inversion and plate areas.

40. A method as in Claim 38 wherein the adjusting step involves adjusting the ratio of the inversion area to the plate area in order to achieve at least a specified value of the ratio of the maximum capacitance to the minimum capacitance.
41. A method as in Claim 38 wherein the selecting act includes configuring the body region to substantially laterally surround, and extend below substantially all of, the plate region.
42. A method as in Claim 38 wherein the selecting and adjusting acts include configuring the plate region to comprise a main plate portion and at least one finger portion continuous with the main plate portion, extending laterally away from the main plate portion, and meeting the body region therealong.
43. A method as in Claim 38 wherein the gate electrode is at a gate-to-body bias voltage relative to the body electrode, the method further including maintaining the gate-to-body voltage approximately constant as the plate-to-body voltage is varied.
44. A method as in Claim 38 wherein the gate electrode is at gate-to-body bias voltage relative to the body electrode, the method further including causing the gate-to-body voltage to differ from the plate-to-body voltage and to vary as a function of the plate-to-body voltage as the plate-to-body voltage is varied.
45. A method as in Claim 44 wherein the causing act entails causing the gate-to-body voltage to vary approximately linearly with the plate-to-body voltage.
46. A method as in Claim 44 wherein the gate-to-body voltage differs by approximately a constant non-zero amount from the plate-to-body voltage.
63. A structure comprising:
a varactor comprising (a) a plate region and a body region of a semiconductor body, (b) a plate electrode and a body electrode respectively connected to the plate and body regions, (c) a dielectric layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body

regions meeting each other to form a p-n junction, a surface depletion region of the body region extending along the dielectric layer below the gate electrode and being spaced apart from a body contact portion of the body region, the body contact portion contacting the body electrode and being more heavily doped than the surface depletion region, the plate region comprising a main plate portion and at least one finger portion continuous with the main plate portion, extending laterally away from the main plate portion, and meeting the body region therealong; and

electronic circuitry having a capacitance signal path for receiving the varactor to enable the circuitry to perform an electronic function dependent on the varactor, the plate and body electrodes being situated in the capacitance signal path.

64. A structure as in Claim 63 wherein each finger portion is of lesser average dimension perpendicular to that finger portion than is the main plate portion.

65. A structure as in Claim 63 wherein there are at least two finger portions.

66. A structure as in Claim 63 wherein there are at least four finger portions.

67. A structure as in Claim 63 wherein the varactor includes a plate electrode and a body electrode respectively connected to the plate and body regions, an inversion layer that meets the plate region selectively appearing and disappearing in the body region below the gate electrode as a plate-to-body bias voltage applied between the plate and body electrodes is varied during operation of the varactor.

68. A structure as in Claim 65 wherein at least two of the finger portions extend longitudinally non-parallel to another.

109. A structure comprising:

a varactor comprising (a) a plate region and a body region of a semiconductor body, (b) a plate electrode and a body electrode respectively connected to the plate and body regions, (c) a dielectric layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions meeting each other to form a p-n junction and extending to a primary surface of the

semiconductor body, a field insulating region extending into the semiconductor body along the primary surface to define a semiconductor island laterally surrounded by the field insulating region and substantially fully occupied by material of the plate and body regions; and

electronic circuitry having a capacitance signal path for receiving the varactor to enable the circuitry to perform an electronic function dependent on the varactor, the plate and body electrodes being situated in the capacitance signal path.

110. A structure as in Claim 109 wherein the plate region occupies a lateral plate area along the primary surface, the varactor has a minimum capacitance dependent on the plate area, the semiconductor island occupies a lateral island area along the primary surface, and the varactor has a maximum capacitance dependent on the island area.

111. A method as in Claim 110 wherein the minimum capacitance is approximately proportional to the plate area, and the maximum capacitance is approximately proportional to the island area.

112. A structure as in Claim 109 wherein the plate region is a substantially unitary region.

113. A structure as in Claim 109 wherein the field insulating region substantially laterally surrounds at least one further semiconductor island occupied by material of the body region substantially up to the primary surface such that material of the body region extends continuously from each semiconductor island to each other semiconductor island.

114. A structure as in Claim 109 wherein the plate region comprises a main plate portion and at least one finger portion continuous with the main plate portion, extending laterally away from the main plate portion, and meeting the body region therealong.

115. A structure as in Claim 109 wherein an inversion layer that meets the plate region selectively appears and disappears in the body region below the gate electrode as a plate-to-body bias voltage applied between the plate and body electrodes is varied during operation of the varactor.

116. A structure as in Claim 109 wherein the plate electrode is at a plate-to-body bias voltage relative to the body electrode, the gate electrode is at a gate-to-body bias voltage relative to the

body electrode, and the gate-to-body voltage is maintained approximately constant as the plate-to-body voltage is varied.

129. A structure as in Claim 116 further including componentry for maintaining the gate-to-body voltage approximately constant at the non-zero value.

117. A structure as in Claim 109 wherein the plate electrode is at a plate-to-body bias voltage relative to the body electrode, the gate electrode is at a gate-to-body bias voltage relative to the body electrode, the gate-to-body voltage differs from the plate-to-body voltage, and the gate-to-body voltage is varied as a function of the plate-to-body voltage as the plate-to-body voltage is varied.

130. A structure as in Claim 117 further including componentry for causing the gate-to-body voltage to vary as a function of the plate-to-body voltage.

118. A structure as in Claim 117 wherein the gate-to-body voltage varies approximately linearly with the plate-to-body voltage.

119. A structure as in Claim 117 wherein the gate-to-body voltage differs by approximately a constant non-zero amount from the plate-to-body voltage.

120. A structure as in Claim 109 wherein the gate electrode is situated outside the capacitance signal path.

121. A structure as in Claim 109 wherein the circuitry includes an inductor situated in the capacitance signal path with the plate and body electrodes to form an oscillatory inductive-capacitive combination whereby the capacitance signal path is an inductance-capacitance signal path.

122. A structure as in Claim 121 wherein the gate electrode is situated outside the inductance-capacitance signal path.

95. A method comprising:

selecting a varactor which comprises (a) a plate region and a body region of a semiconductor body, (b) a dielectric layer situated over the semiconductor body and contacting

the body region, (c) a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, and (d) a plate electrode and a body electrode respectively connected to the plate and body regions, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions meeting each other to form a p-n junction and extending to a primary surface of the semiconductor body, the plate region occupying a lateral plate area along the primary surface, a field insulating region extending into the semiconductor body along the primary surface to define a semiconductor island laterally surrounded by the field insulating region and substantially fully occupied by material of the plate and body regions, the semiconductor island occupying a lateral island area along the primary surface, the varactor having a maximum capacitance dependent on the island area; and

adjusting the plate and island areas to control the minimum and maximum capacitances of the varactor.

96. A method as in Claim 95 wherein the minimum capacitance is approximately proportional to the plate area, and the maximum capacitance is approximately proportional to the island area.

97. A method as in Claim 95 wherein the selecting act includes configuring the plate region to be a substantially unitary region.

98. A method as in Claim 95 wherein the selecting act includes configuring the field insulating region to substantially laterally surround at least one further semiconductor island occupied by material of the body region substantially up to the primary surface such that material of the body region extends continuously from each semiconductor island to each other semiconductor island.

99. A method as in Claim 95 wherein the selecting and adjusting acts include configuring the plate region to comprise a main plate portion and at least one finger portion continuous with the main plate portion, extending laterally away from the main plate portion, and meeting the body region therealong.

100. A method as in Claim 95 wherein an inversion layer that meets the plate region selectively appears and disappears in the body region below the gate electrode as a plate-to-body

bias voltage applied between the plate and body electrodes is varied during operation of the varactor.

101. A method as in Claim 95 wherein the gate electrode is at a gate-to-body bias voltage relative to the body electrode, the method further including maintaining the gate-to-body voltage approximately constant at a non-zero value as the plate-to-body voltage is varied.

102. A method as in Claim 95 wherein the gate electrode is at gate-to-body bias voltage relative to the body electrode, the method further including causing the gate-to-body voltage to differ from the plate-to-body voltage and to vary as a function of the plate-to-body voltage as the plate-to-body voltage is varied.

103. A method as in Claim 102 wherein the causing act entails causing the gate-to-body voltage to vary approximately linearly with the plate-to-body voltage.

104. A method as in Claim 102 wherein the gate-to-body voltage differs by approximately a constant non-zero amount from the plate-to-body voltage.

105. A method as in Claim 95 further including providing electronic circuitry having a capacitance signal path for receiving the varactor to enable the circuitry to perform an electronic function dependent on the varactor, the plate and body electrodes being situated in the capacitance signal path.

106. A method as in Claim 105 wherein the gate electrode is situated outside the capacitance signal path.

107. A method as in Claim 95 further including providing electronic circuitry comprising an inductor situated in an inductance-capacitance signal path with the plate and body electrodes to form an oscillatory inductive-capacitive combination.

108. A method as in Claim 107 wherein the gate electrode is situated outside the inductance-capacitance signal path.